ENGG1000
Engineering Design and Innovation

Session 1, 2012

Supplementary Details for Projects in the School of Electrical Engineering and Telecommunications

Introductory Note
ENGG1000 is a single course coordinated by the Faculty of Engineering. Most of the course is run by individual schools within the Faculty, through a collection of structured projects. This document provides supplementary information which is specific to projects undertaken within the School of Electrical Engineering and Telecommunications (EE&T); it is intended to be read in conjunction with the faculty-wide course outline, which you should have received in the first lecture, but may also obtain via Moodle (https://moodle2.telt.unsw.edu.au/login/index.php).

Course Staff within the School of EE&T
EE&T Project Coordinator: Dr Julien Epps
Office: EE337    Phone: 9385 6579    Email: j.epps@unsw.edu.au
Consultation times: Dr Epps will be available during most scheduled laboratory times, and is also available for consultation from 5pm to 5:45pm on Mondays and Thursdays during the semester (either in the lab or the office). Due to his joint appointment with National ICT Australia, Dr Epps may not be in his office on other days.

Staff Mentors: Each student will be assigned to an individual mentor group, with guidance from members of academic staff. 15% of the marks are derived from your mentor’s assessment of your learning and participation.

Laboratory Demonstrators: Each laboratory will be staffed by a number of experienced demonstrators.

Course details
Credits: The course is a 6 UoC course; expected workload is 10 hours per week throughout the 13 week session.

Contact hours: The course comprises lectures, mentor meetings and laboratory work up to 5-6 hours per week, depending on the activities scheduled in each week (refer to schedule below in this outline and also the faculty-wide schedule in the Faculty ENGG1000 Course Outline).

Lectures: Webster Theatre A (Mondays 2-3pm) and OMB149 (Thursdays 2-3pm), starting Thursday, Week 2. Note that there will also be some faculty-run lectures in various locations through the course. See the calendar for more information.
**Laboratories:** Mondays 2-5:30pm, in EE101/102/113/114, all on the 1st floor of the EE building.

**Mentor Group Locations:** Various locations – see the ElecEng project web site http://engg1000.ee.unsw.edu.au and/or the faculty online teaching site Moodle (https://moodle2.telt.unsw.edu.au/login/index.php) in Week 2 for more details.

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**Course Information**

**Aims within the School of EE&T**

The main aims of ENGG1000 are clearly explained in the Faculty Course Outline. In keeping with these, the EE&T project aims to provide a framework for experiential learning, to introduce you to the design process, and to familiarize you with the many facets of engineering projects. Within the school, however, there are some specific additional aims:

- **a.** To convey some basic details of the principles of electrical devices, construction of electronic circuits and analysis techniques, in order to design, build and test simple circuits.
- **b.** To familiarize you with the test equipment available in the electronics laboratories, in order to evaluate your design effectively.
- **c.** To motivate the learning you will undertake in future courses, both in science and engineering, through a practical design problem.

Perhaps unlike some other projects in ENGG1000, many students may not begin the course with much experience in building circuits or measuring electrical quantities. This course provides a fairly gentle (and hopefully fun!) introduction to electronic circuits, while keeping the emphasis on engineering design.

It is not the aim of this course to provide a detailed understanding of electronics. A common question is why so many complex devices and circuits are introduced. The answer is simple: purely resistive circuits are not interesting as design projects. The technical stream of this course tries to give the minimal detail required in order to use a wide array of different kinds of circuits, while mastery is left for later courses.

**Learning outcomes**

Additionally to the faculty learning outcomes, on successful completion you should be able to:

1. Appreciate some of the design challenges faced by electrical and telecommunications engineers, and what kinds of skills and knowledge are needed to tackle them.
2. Give examples of design trade-offs typically experienced during electrical design.
3. Explain the types of applications of simple electronic circuits, and suggest circuit designs for simple problems.
4. Understand basic electrical quantities, in particular voltage and current, from a practical perspective: how to measure them and what values to expect for a given circuit design or application.
5. Suggest approaches for debugging simple circuit problems.

Teaching strategies
The teaching strategies are explained in more detail in the faculty course outline. Like other projects, the teaching in the EE&T component of this course is centred around the project. For example, you will develop communication skills by communicating about the project; you will develop teamwork and project management skills in endeavouring to accomplish your project on time; you will experience the kinds of technical problems that engineers deal with on industrial projects; you will learn the importance of identifying sub-systems within a design and planning carefully for their integration by solving a complex problem; you will develop design skills by following a design process, by evaluating and comparing designs and by reflecting on them; you will learn information literacy as you sift through large amounts of information to focus in on exactly what you need to propose and implement your design. Although other courses in your degree may vary in their teaching strategy, your understanding of and ownership of the learning process developed in this course should prove invaluable for the remainder of your degree program.

The course consists of lectures, labs and tutorials. The lectures will provide the rationale for the design process followed in the course and some basic electrical engineering principles to act as a starting point for addressing the design brief. The labs and mentor meetings are intended to provide guidance on your self-directed path of discovering the relevant information and skills needed to successfully complete the project.

Mentor meetings in particular have been found to provide a very effective means of transferring knowledge and guidance. Each project team, of approximately 8 students, meets with an academic staff mentor for 1 hour in each of weeks 2 through 12. Mentors facilitate discussions of the design process and help you to reflect upon your learning in the course. Mentors will expect to see your laboratory notebooks and discuss your design ideas with you, and will expect to see teams meeting regularly, developing action points for team members, and follow-up on these by individuals. Mentors can help you to understand design concepts, background knowledge in electronic circuits, and many other things, but you need to take the initiative to use this resource by coming prepared to your mentor meetings, with questions. Mentors can also help to put the role of other classes such as Maths and Physics into perspective with respect to engineering design. Mentors will assess your individual learning and contribution to your team’s design project. Your design proposal will be marked by your own mentor, but your final report will be marked by another group’s mentor. This provides calibration data to help equalize scores given by different markers and also motivates you to write clearly for others to read your work.

Relation to other courses
Within the School of EE&T there are courses on design and innovation at nearly every level of the curriculum: in third year, ELEC3117 is a design course in which a substantive project is undertaken, while in fourth year, ELEC4123 builds on students’ design proficiency and in most cases design is an aspect of the final year honours project. ENGG1000 can thus be seen as an introduction to a design theme that runs throughout
electrical/telecommunications/photonics engineering. ENGG1000 also provides introductory-level knowledge of aspects of electrical energy, electronics, telecommunications and control systems, which together form the majority of courses within the EE&T degree programs.

**Assessment Specific to the ElecEng Project**
Assessment in the ElecEng project has similar components to the other projects throughout ENGG1000, however an effort has been made to keep the number of assessments to a minimum, to provide a positive learning experience and in response to student feedback from previous semesters. This is made possible largely through the mentoring process.

<table>
<thead>
<tr>
<th>Assessment</th>
<th>Weight</th>
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<tbody>
<tr>
<td>Faculty-wide design process (individual)</td>
<td>5%</td>
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<tr>
<td>Laboratory skills test (individual)</td>
<td>10%</td>
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<tr>
<td>Circuit design principles test (individual)</td>
<td>10%</td>
</tr>
<tr>
<td>Active learning, planning and participation, assessed by mentors (individual: 7.5%, group: 7.5%)</td>
<td>15%</td>
</tr>
<tr>
<td>Lab notebooks, assessed by mentor and lecturer (individual)</td>
<td>10%</td>
</tr>
<tr>
<td>Design proposal report, marked by the mentor (group)</td>
<td>10%</td>
</tr>
<tr>
<td>Acceptance testing, marked by the lecturer (group)</td>
<td>10%</td>
</tr>
<tr>
<td>Final testing, marked by the lecturer (group)*</td>
<td>10%</td>
</tr>
<tr>
<td>Final design report, marked by a different mentor (group)*</td>
<td>20%</td>
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* This mark is moderated by peer assessment (see below)

The assessment is thus roughly evenly distributed between individual and team marks, reflecting the requirement of the project. Experience from previous semesters shows that well-organised groups that communicate, set high standards, self-organise and resolve conflicts effectively are essential to succeeding in the project.

The laboratory skills test will assess your familiarity with basic circuit construction and analysis and laboratory equipment, gained while completing the introductory labs (which are otherwise non-assessable), and will give you feedback on your understanding of these. Marks will be assigned by lab demonstrators according to predetermined criteria.

The circuit design principles test will assess your understanding of simple circuit analysis and design using a written exam of 30 min duration. Marks will be assigned based on the correctness of your answers.

The learning, planning and participation mark will be assigned by your mentor. High marks will be given for the following:
- Individual: Committed to project, actively contributing to mentor meetings and non-timetabled meetings, to the design and its implementation and testing, and to the written submissions. Demonstrates commitment to the success of the group (as defined by the group at the beginning of the project) and helps the group to function effectively.
• Group: Has clear goal that everyone follows. Generates, records and follows up action points from meetings (which should be held regularly outside of timetabled hours). Works well together. Is motivated. Can resolve conflicts effectively. Generates a realistic and detailed plan that everyone sticks to (revisions agreed by the group are allowed). Marks above 3.5/7.5 can only be expected by groups who are meeting regularly outside of the designated lab and mentor times.

Lab notebooks are a means of recording design, technical and organizational information for later use, and are a helpful tool both during study and in professional life. You must bring your lab notebook to all classes, and record both the introductory lab and notes from mentor meetings and later labs. Lab notebooks will be assessed according to the following criteria: purpose of notes (why were they made?), date (when were they made?), clarity (could someone else understand them?), detail (e.g. if you sketch your circuit diagram, could someone else build it exactly from the sketch?), completeness of experimental notes, interpretation of results or discussion of design/circuit, and evidence of research or individual input (i.e. repeating lecture notes will not attract marks). Marks will be assigned in week 12, but the lecturer or mentor may request your notebook at any time.

Written communication is consistently among the top priorities for engineering employers, and developing report writing skills are an important aspect of design and innovation. The criteria for assessing the design proposal and final design reports are given on the respective report cover sheets.

The acceptance testing and final testing assess the success of the group’s solution to the given problem. The details and marking criteria used during the testing are given in the ElecEng project brief.

The final testing and final report marks will be moderated on an individual basis by peer assessment. Peer assessment will be conducted as follows:

• During the mentor meeting after the acceptance testing, you will score all your fellow team members on their contribution to the project. This feedback will be anonymously passed to them, and the scores will not be used for assessment purposes.

• At the final mentor meeting, you will again score all your fellow team members on their contribution to the project. The scores of your team members will be averaged to produce a peer assessment score for the project. This score will then be used to moderate the final testing and final report marks, i.e. if you contribute little to the team, then your final testing and final report marks may be lower than for others in the team, while if you are a strong contributor to the team, then your final testing and final report marks may be higher than for others. The peer assessment will be applied as an individual weighting to the final testing and final report group marks.

Peer assessment is an important part of assessing group projects, because your contribution to the team is vital to the team’s success.

Late submissions of assessed work attract a penalty of 5% per day, including weekends. After 10 days, a mark of zero will be awarded.
Course Schedule

<table>
<thead>
<tr>
<th>Week</th>
<th>Monday</th>
<th>Thursday</th>
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<tbody>
<tr>
<td>1</td>
<td>2:00 Introductory lecture (Clancy Auditorium or Science Theatre)</td>
<td>2:00 Impromptu design (assessable) – see faculty outline. Venues advised at Monday Week 1 lecture or online</td>
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<tr>
<td>2</td>
<td>2:00 Review impromptu design (assessable) – see faculty outline</td>
<td>2:00 Lecture 1 (OMB149) 3:00-4:00 or 4:00-5:00 Mentor meeting 1</td>
</tr>
<tr>
<td>3</td>
<td>2:00 Lecture 2 (Webster Th. A) 3:00-5:30 Laboratory*</td>
<td>2:00 Lecture 3 (OMB149) 3:00-4:00 or 4:00-5:00 Mentor meeting 2</td>
</tr>
<tr>
<td>4</td>
<td>2:00 Lecture 4 (Webster Th. A) 3:00-5:30 Laboratory*</td>
<td>2:00 Lecture 5 (OMB149) 3:00-4:00 or 4:00-5:00 Mentor meeting 3 Submit project plan to mentor</td>
</tr>
<tr>
<td>5</td>
<td>2:00 Lecture 6 (Webster Th. A) 3:00-5:30 Laboratory*</td>
<td>2:00 Lecture 7 (OMB149) 3:00-4:00 or 4:00-5:00 Mentor meeting 4</td>
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<tr>
<td></td>
<td>Mid-semester break</td>
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<tr>
<td>6</td>
<td>2:00-5:30 Laboratory skills test*</td>
<td>2:00 Lecture 8 (OMB149) 3:00-4:00 or 4:00-5:00 Mentor meeting 5</td>
</tr>
<tr>
<td>7</td>
<td>2:00-5:30 Laboratory*</td>
<td>2:00 Lecture 9 (OMB149) 3:00-4:00 or 4:00-5:00 Mentor meeting 6</td>
</tr>
<tr>
<td>8</td>
<td>2:00-5:30 Laboratory*</td>
<td>2:00 Circuit design principles test (OMB149) 3:00-4:00 or 4:00-5:00 Mentor meeting 7</td>
</tr>
<tr>
<td>9</td>
<td>2:00-5:30 Laboratory*</td>
<td>2:00 Acceptance testing (EE319)</td>
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<tr>
<td>10</td>
<td>2:00-5:30 Laboratory*</td>
<td>2:00 Lecture 10 (OMB149) 3:00-4:00 or 4:00-5:00 Mentor meeting 8</td>
</tr>
<tr>
<td>11</td>
<td>2:00-5:30 Laboratory*</td>
<td>2:00 Lecture 11 (OMB149) 3:00-4:00 or 4:00-5:00 Mentor meeting 9</td>
</tr>
<tr>
<td>12</td>
<td>2:00-5:30 Laboratory*</td>
<td>2:00 Lecture 12 (OMB149) 3:00-4:00 / 4:00-5:00 Mentor meeting 10</td>
</tr>
<tr>
<td>13</td>
<td>2:00-5:00 Final testing (EE319)</td>
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*EE101, 102, 113, 114
Yellow shading denotes Faculty of Engineering activities

Key dates

**Week 1 (Friday):** By now you must have selected your project, by following the instructions on Moodle (https://moodle2.telt.unsw.edu.au/login/index.php)

**Week 4 (Mentor meeting):** Submit a project plan to your mentor. This is not assessable, but is your first opportunity for formal feedback.

**Week 6 (Mentor meeting):** Submit one design proposal per sub-group (i.e. three separate reports) to your mentor.

**Week 13 (Friday):** Submit your team’s final report (2 copies) to the assignment drop-box outside room EEG12. Ensure that the cover sheet has been signed by all team members and that your ‘mine’ has been returned to the lecturer.
Resources
Wondering where or how to get started? Here are some suggestions, from various sources:

- The recommended text book for ENGG1000:

- Another good one for introductory engineering design is:

- More specifically for electrical engineering design are:
  - Wilcox, A. D., *Engineering Design for Electrical Engineers*, Pearson/Prentice-Hall, 1989 (this interprets design perhaps more closely to EE&T than the others, and in various sections discusses aspects of specific relevance to Electrical Engineering)

- More technical books that may help (most helpful in bold) include:
  - Brindley, K., *Starting Electronics*, Elsevier, Burlington, MA, 2005. (very clearly written, this is an excellent introduction to electronics for anyone new to the subject) – in UNSW library
  - Scherz, P., *Practical Electronics for Inventors*, McGraw-Hill, 2000 (this is a very helpful book on introductory electronics, and includes example circuits and practical design tips) – in UNSW library
  - Carlson, A. B., and Gisser, D. G., *Electrical Engineering: Concepts and Applications* (this is not a design text, but is written at about the right level to provide a useful resource for circuit analysis)

- Also:
  - The EE&T project web site [http://engg1000.ee.unsw.edu.au](http://engg1000.ee.unsw.edu.au) (may be updated as the semester unfolds)
Selinger, C., *Stuff you don’t learn in engineering school: Skills for success in the real world*, Wiley, 2004 (how to work in a team, etc. Read it for interest, or before you do your industrial training)


Circuit example web sites, for example:

- [http://www.aldinc.com/ald_circuitideas.htm](http://www.aldinc.com/ald_circuitideas.htm)
- [http://www.discovercircuits.com/list.htm](http://www.discovercircuits.com/list.htm)
- [http://www.allaboutcircuits.com/](http://www.allaboutcircuits.com/)
- [http://www.opencircuits.com/Basic_Circuits_and_Circuit_Building_Blocks](http://www.opencircuits.com/Basic_Circuits_and_Circuit_Building_Blocks)
- [http://www.kpsec.freeuk.com/trancirc.htm](http://www.kpsec.freeuk.com/trancirc.htm)
- [http://hobby_elec.piclist.com/e__pic.htm](http://hobby_elec.piclist.com/e__pic.htm) (PIC microcontrollers)

**Preparation for Laboratories**

You are advised to do the following in preparation for your first electronics laboratory:

- Wear covered shoes. Without these you will be refused entry to all Electrical Engineering labs.
- Obtain a prototyping board before the first lab. If you do not own one, you can purchase one from the Electrical Engineering School Office for $15.
  - You may also find it helpful to have a small pair of pliers and a set of small screwdrivers.
- Get a lab notebook, and bring it to every lab (and every mentor meeting and team project meeting).
- Read the laboratory exercises in advance of the lab.
- Read the related lecture notes in advance of the lab, and bring them to the lab.
- If you expect to do soldering (more likely in the later labs), bring safety goggles or purchase them from the Electrical Engineering School Office for $5.

The Electronics Workshop is located in room G15, on the ground floor of the Electrical Engineering building. The staff in the Electronics Workshop are very friendly and helpful. Any of the components whose datasheets appear on the course web site at [http://engg1000.ee.unsw.edu.au](http://engg1000.ee.unsw.edu.au) may be obtained from the Electronics Workshop free of charge, although limits may apply to the quantities you can request. You should, however, bring a component request form, signed by one of the laboratory demonstrators. This form may also be found on the course web site.
Other Matters

Academic Honesty and Plagiarism
Plagiarism is the unacknowledged use of other people's work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a serious offence by the University and severe penalties may apply. Instances of plagiarism are detected in submitted work in the ENGG1000 ElecEng project virtually every year, and penalties are applied. For more information about plagiarism, please refer to http://www.lc.unsw.edu.au/plagiarism, or seek advice from course staff.

Continual Course Improvement
The course is under constant revision in order to improve the learning outcomes of its students. Many positive comments have been received about the EE&T project stream of ENGG1000 in previous years, and all successful aspects of the course have been retained. In 2012, modifications due to student and/or staff feedback include: (i) NEW: many downloadable pre-recorded worked examples, (ii) improved group-based activities designed to improve/catalyse team cohesion and effectiveness, (iii) explaining the mentor process better, (iv) live peer assessment to give feedback to other team members and moderate group assessments, and (v) new group participation requirements in the acceptance testing assessment. Please forward any feedback (positive or negative) on the course to the course convener or via the Course and Teaching Evaluation and Improvement Process (surveys at the end of the course).

Administrative Matters
On issues and procedures regarding such matters as special needs, equity and diversity, occupational heath and safety, enrolment, rights, and general expectations of students, please refer to the School policies, see http://scoff.ee.unsw.edu.au/.

Acknowledgements
Parts of some materials for this course were developed by Prof. D. Taubman or Dr C. Reidsema, both of whom have contributed greatly to the development of this course since its inception.