ENGG1000: Engineering Design and Innovation
Stream: School of EE&T

Dalek Enemy Target: Functional Description

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1 Purpose

A very cursory description of the Dalek enemy target is found in the School of EE&T’s project overview document. At the opposite extreme, the complete circuit schematic and PCB layout for the enemy target you are being given may be found on the course web-site. The purpose of the present document is to bridge the gap between these two sources of information, providing you with a comprehensive yet easily read description of what the enemy target does. This is important, of course, because the objective of your design project is to detect the location of the enemy target, orient your plunger to face it, and then emit an “exterminate” message. It is likely that sub-group SG-B will have a greater interest in this description, since they are primarily responsible for the detection problem. However, all team members should at least familiarize themselves with what they are up against as a team.

2 Signals Produced by the Enemy Target

Each enemy target contains an on-board signal generator, which continuously generates the “CLK” and “WAVE” signals shown in Figure 1, whenever power is applied. These exact same signals may be recovered via the stereo “heartbeat” jack, which is on the side of the printed circuit board (PCB), furthest from the battery. In Week 5, you will be supplied with a 3.5mm plug that you can insert into this jack and use to observe the signals on the laboratory oscilloscopes. We suggest that you do this early, so that you can verify which pin is which. Note that the two heartbeat signals are both referenced to the common “GND”

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1 As noted elsewhere, the “exterminate” message may be anything from a visible light, to an auditory tone, or even a reproduction of the original Dalek “exterminate” message.

2 Power is applied when the battery switch is on. If your battery runs down, you can remove it and apply 9V from lab power supplies, via the red and black banana plugs. However, we recommend that you always operate from the battery.
Figure 1: The two heartbeat signals produced by the enemy target.

terminal, which is the outermost connector on the stereo plug. If in doubt, ask a demonstrator, or experiment to find out which is which.

All signals are at TTL levels, which simply means that they are suitable for supplying directly to pretty much any logic IC you will get your hands on. There are only two signal levels of interest: low (close to GND = 0V); and high (approximately 4V). Infrared LED turns “on” when the CLK and WAVE signals are different – i.e., when one is low and the other is high. The loudspeaker is driven by an efficient power amplifier which takes its input directly from the WAVE signal.

The CLK signal cycles from low to high and back to low again at roughly 20 kHz (20 thousand times per second). Note carefully, though, that the actual frequency may vary considerably from one enemy target to another. The reason for this is that the exact frequency of oscillation depends upon the values of resistors R1 and R2 and capacitor C2. These values are nominally the same for all enemy targets, but actual component values vary within manufacturing tolerances. Manufacturing tolerances for the resistors are ±5%, while manufacturing tolerances for the capacitor are ±20%. Despite this variation, when multiple daleks are connected together via the “Daisy-Chain-In” and “Daisy-Chain-Out” ports, they will all share the same heartbeat – that of the first target in the chain.

3 Safe Use of your Enemy Target

3.1 Powering it up

We ask you to always power your enemy target via the 9V battery. It is possible to supply power separately via the red and black banana plugs, but you MUST NOT DO THIS unless you first disconnect the battery. If you are in any doubt, ask a demonstrator. Also, if you do supply external power, you should ensure that the voltage is close to 9V (no more than 12V!).
3.2 Physical Care

Don’t get it wet. Be particularly careful of the exposed PCB (Printed Circuit Board), since you could damage the components. Try to keep the PCB free from dust and grime, which could potentially provide unwanted conductive paths. Leave the battery in the “off” position when not in use, since there is a small but constant current drain when the battery is in the “on” position.

3.3 Interfacing to the Heartbeat Signal (if required)

You should note that the signals put out over the “heartbeat” jack are buffered through a 74LS244 IC. Whatever load you apply to these signal lines in your dalek should not affect the behaviour of the enemy target or other enemy targets with which it may be inter-connected for final testing. The outputs from this buffer IC are delivered via a pair of 470Ω resistors. These help to prevent you from damaging the circuit and also to limit the rate at which signals may change in any cable attached to the heartbeat jack. This will be discussed more in lectures, in connection with capacitors.

You should be careful to ensure that your dalek does not apply voltages outside the range $-0.5\,\text{V}$ to $+5.5\,\text{V}$ to either of the heartbeat signal lines, measured relative to GND. The best way to achieve this is to bring the heartbeat signals into your dalek via a 74LS244 IC of your own, following the pattern you can see in the enemy target schematic diagram. To do this, you should first obtain a 74LS244 from the electronics workshop and arrange for it to be powered by 5V. Use the datasheets to find out which pins are which. To obtain a 5V power source, you might use a voltage regulator based around the 7805. Again, you can use the enemy target schematic as a template for how you might do this, but also consult your lecture notes. It is fine to connect the enemy target signal lines directly to any of the 8 buffer input pins on your 74LS244, being careful to ensure that the signal GND is connected to the GND power pin on the 74LS244. This IC has specially designed input circuitry to remove noise from its input signals, but for absolutely clean signals you should also connect a small capacitor (e.g., 10 nF) between GND and each of the heartbeat signals. These capacitors will slow the signals down a little bit – something you can observe on the CRO – but “filter out” a lot of unwanted noise.

4 Description of Individual Sub-Systems

4.1 Generation of the “Heartbeat”

The internal heartbeat signals (INT-CLK and INT-WAVE) are generated by IC’s U2 and U3. U2 is a LM555 timer/multi-vibrator chip. You might like to consult the manufacturer’s datasheets, available via the course web-page, where you will find both a description of the chip and some typical applications, including the oscillator application implemented here. Basically, resistors R1 and R2 are used to alternately charge and discharge capacitor C2. More specifically,
resistor R2 initially charges capacitor C2, so that its voltage gradually rises towards the 5V voltage rail (VCC). At some point the threshold detector in U2 observes that the voltage at pin 6 has risen above an internal upper threshold \( T_U \), which causes the chip to enter the discharge mode. In the discharge mode, pin 7 is pulled down close to ground by an internal NPN transistor. This acts to discharge the capacitor until the voltage at pin 2 (same as that at pin 6 here) reaches an internal lower threshold \( T_L < T_U \), at which point the charging process recommences. The output at pin 3 of U2 alternates between low (close to GND) and high (close to VCC), depending on whether the chip is in the charging or discharging phase.

There are a couple of points worth observing in regard to the oscillator implemented via U2, R1, R2 and C2. Firstly, the amount of time spent charging is not identical to that spent discharging. One reason for this is that the charging process involves only R2, whereas the discharging process involves R1 working against R2. Secondly, the frequency of oscillation depends upon the resistor and capacitor values as well as the voltage thresholds \( T_L \) and \( T_U \). All of these values vary somewhat from component to component.

The \( Q \) output (pin 3) from U2 forms the INT-CLK signal. The internal INT-WAVE signal is generated by a 4-bit counter, U3. Digital logic, including counters, will be described later in the lecture program. For now, all you need to know is that the count appears as a 4 digit binary number of QA (units), QB (twos), QC (fours) and QD (eights). The count increments on the rising edge (low \( \rightarrow \) high) of the CLK input (pin 2). When the count reaches 15 (the maximum 4 digit binary number), the next rising edge of the CLK signal sends it back to 0. Accordingly, the QD value (pin 11) is low for the first 8 counts, high for the next 8 counts, then low for the next 8 counts, and so forth. This becomes the INT-WAVE signal.

The INT-CLK and INT-WAVE signals pass through buffers (74LS244) to form what are known as BUS-CLK and BUS-WAVE. In the standalone mode, these bus signals are slightly delayed versions of INT-CLK and INT-WAVE, where the delay is introduced by resistor-capacitor networks which serve to slow down the rate at which the signals rise or fall. Slower signals produce less electromagnetic interference sent over external cables. In the event that enemy targets are daisy-chained together, the bus signals are formed from those arriving at the “Daisy-Chain-In” jack J1, where they are further slowed down by resistor-capacitor networks. The main purpose here is to filter out noise.

The filtered BUS-CLK and BUS-WAVE signals are sent through buffers once again to form the CLK and WAVE signals of the heartbeat. The CLK signal is used to drive the infrared LED, as described in Section ???. The WAVE signal is used to drive the speaker, as described in Section ???.

4.2 Driving the Infrared LED

The U5 chip contains four XOR (exclusive OR) logic gates. The XOR function produces logic level 1 (high) if and only if the two inputs are different (one high and one low). Accordingly, when CLK and WAVE differ, the base of transistor
T1 is supplied with current via R3. Noting that a logic high corresponds to around 4V or more, the base current to T1 satisfies

\[ i_B \geq \frac{4 - 0.6}{R3} = 0.34 \text{ mA} \]

If T1 does not saturate, its collector current will be equal to \( \beta \cdot i_B \), where \( \beta \geq 100 \) is the current gain. This would suggest a collector current of more than 300 mA, which actually exceeds the transistors maximum rated collector current of 200 mA. However, looking at the output side of the transistor, we see that the collector current cannot exceed \( V_{R4}/R4 \), where \( V_{R4} \) is the voltage across resistor R4. Clearly \( V_{R4} \) must be less than 9V, so the collector current must be less than 75 mA. We conclude from this that the transistor must go into saturation.

Using typical values of \( V_{sat} \approx 0.4\text{V} \) and \( V_{LED} \approx 1.2\text{V} \) for an infrared LED, we get

\[ V_{R4} \approx 9 - 1.6 = 7.4 \text{ volts.} \]

You can get more accurate values for the transistor saturation voltage and forward LED voltage drop from the manufacturer’s datasheets provided. In any case, the conclusion is that roughly 60 mA will flow in the LED when CLK and WAVE differ. When CLK and WAVE are identical, however, T1 is off and no current flows in the LED.

You may wonder why T1 is required at all. Why did we not just drive the infrared LED directly from the output of U5, via a suitable resistor. To understand why, consult the datasheets\(^3\) and try to find out what maximum output current this device can deliver. Note that the answer is different for source current (current coming out of the pin) to sink current (current flowing into the pin).

### 4.3 Driving the Speaker

The speaker is driven by a so-called “class C” power amplifier, which is designed to pull its output close to one or the other of the power supply rails - i.e., +9V or 0V (GND). In normal operation, exactly one of the two output transistors, T4 and T5, is “on”\(^4\). It is important that T4 and T5 can never be on at the same time; otherwise, a very large current would flow directly from +9V to GND through the two transistors, which would destroy them. Transitors T2 and T3, together with diodes D2 through D6 are designed to ensure that it is not possible for T4 and T5 to be on at the same time.

For the purpose of the discussion here, the output of the amplifier is considered to be the common point at the collectors of T4 and T5. You will note that this common point is connected through to the speaker via an electrolytic capacitor, C3. This capacitor maintains an average charge of 4.5V across its plates. This is because the average current flowing through a capacitor is always

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\(^3\)You might like to just look up the 74LS86, which is a chip we have available for you in the electronics workshop.

\(^4\)By “on,” we mean that it has a non-zero base current.
equal to 0 Amps, which means that the average voltage across the speaker must be 0 Volts; however, the average voltage at the output of the class C power amplifier is 4.5V, since it spends half its time pulled close to GND and half its time pulled equally close to +9V. The purpose of the capacitor C3 is to ensure that all currents flowing in the speaker contribute to sound volume. Adding any constant current to the speaker simply introduces a fixed displacement to its diaphragm, which wastes power but produces no sound. It follows that the most efficient configuration involves an average speaker current of 0.

We turn our attention now to how the circuit works. It is simplest to completely ignore D3, D4, D5, D6, R9 and R10. These components serve only as a backup protection mechanism to limit the amount of current which can flow through output transistors T4 and T5, in the event that the output is accidentally shorted to +9V or 0V. See if you can work out what this maximum current might be after you have first understood the circuit without them. We will also ignore diodes D7 and D8 here. Under normal conditions, these do nothing. They actually serve to protect the output transistors in the event that the speaker pulls the output voltage outside the range of 0V to +9V.5

The simplified circuit is shown in Figure 2. To understand this simplified circuit, consider first the case in which the WAVE signal is in the low state. In this case, transistors T2 and T3 are both off. As a result, T4 must also be off, having no base current, whereas T5 is on, being supplied with a base current via resistor R7.

Now consider the case in which the WAVE signal is in the high state. In this case, current flows through resistors R5 and R6 into the bases of transistors T2 and T3. These base currents cause much larger collector currents to flow. That in T2 flows down via the base of T4 through resistor R8, so that T4 is on. The collector current in T3 comes through R7, diverting it from the base of T5 so that T5 is left in the off state. It is worth noting that both T2 and T3 transistors are saturated here. That is, the actual current which flows in each transistor’s collector is less than the product of its current gain and base current, being limited by R7 or R8, as appropriate. For correct operation, it is important that T3’s saturation voltage is significantly smaller than 0.6V; this is indeed the case.

At this stage, the role of diode D2 is probably still a mystery to you. This diode exists to handle the intermediate cases, when the WAVE signal takes on a value between the low and high state. Admittedly, it only takes a few nano-seconds for WAVE to transition from low to high or high to low, but it is good practice to take steps to ensure that transistors T4 and T5 cannot both simultaneously be on during this transition. The presence of D2 means that no current can flow in the base of T4 until the WAVE voltage exceeds 1.2V.

5 The fact that this can happen may be quite surprising. It is a consequence of the fact that the speaker is actually an electromagnetic, which can generate large “back-voltages” if an attempt is made to change the current quickly. You do not need to worry about the specifics, but it may be useful to know that if you are electronically driving an electromagnetic device, you should always include reverse biased protection diodes, following the pattern of D7 and D8.
so that current can flow in T2. By this stage, the base current in T3 will be $0.6V/47k\Omega \approx 13\mu A$, which is enough to drive it into saturation, keeping T5 off. At saturation, the collector current in T3 is approximately $9V/5.6k\Omega \approx 1.6mA$, so a current gain of 123 or more is sufficient to ensure that T5 is always off whenever T4 is on, no matter what the WAVE voltage might be at any given point in time. According to the datasheets, the BC549 transistor prescribed here has a current gain (HFE) in the range 200 to 800.